Kuldeep Gohil

Professor Tramel

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Lab 7 Report

**Description**: This lab was about implementing a state machine on the Xilinx software. The state machine would consist of inputs, outputs, and state variable to keep track of the steps. The output would be shown through the LEDs on the NEXYS 3 Board.

**What I did:** I copied down the Verilog code provided for the machine module and the pulseit module. I then created a new module titled topLevel module, which assigned all the inputs and outputs to their rightful value. Then, I simulated the work on the NEXYS board by using one switch as the input, one button as the reset, and 3 LEDs as the output. When the switch was not active, the LEDs would go in the pattern of 3, 1, and 2. When the switch was active, the LEDs would go in the pattern 2, 1, and 3. This displays the state of the machine.